FIG. 1

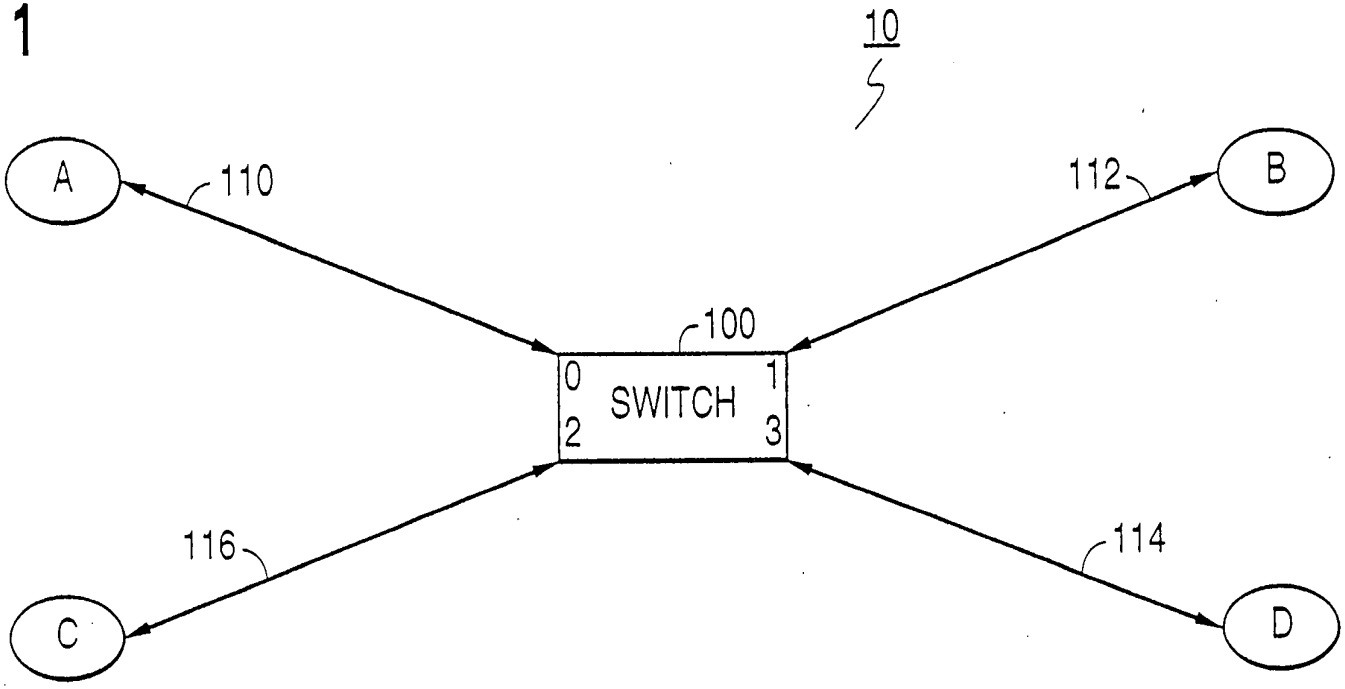

10
A
110
B
112
100
0
1
SWITCH
2
3
116
C
114
D

FIG. 3

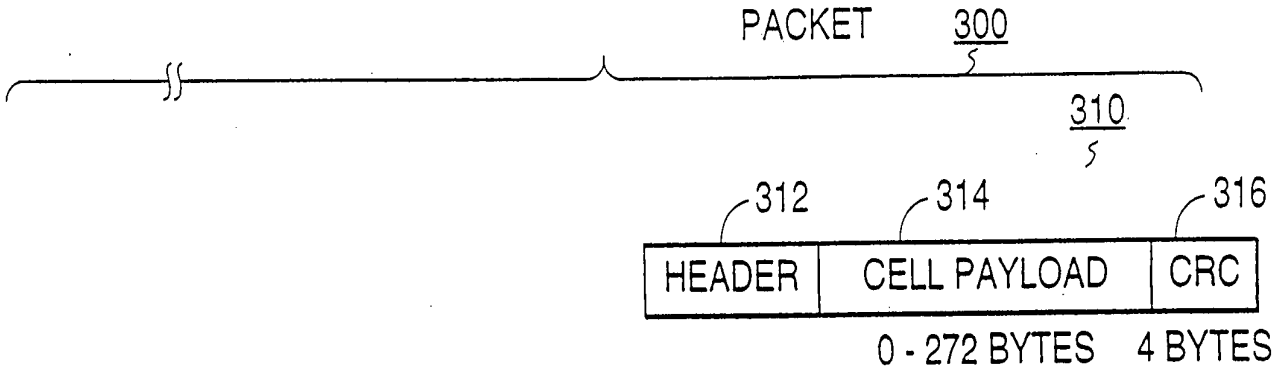
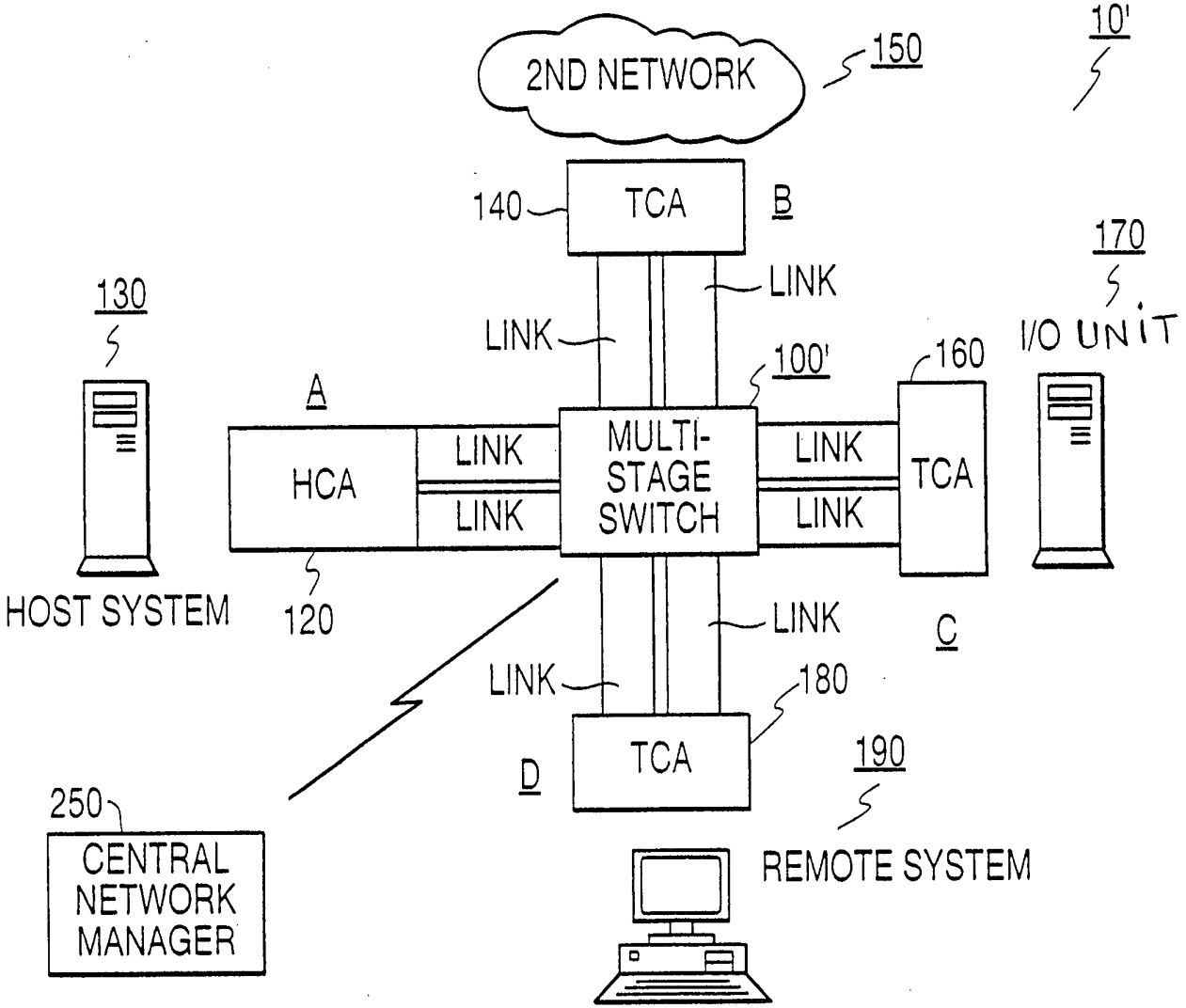

PACKET
300
310
312
314
316
HEADER
CELL PAYLOAD
CRC
0 - 272 BYTES
4 BYTES

FIG. 2


10'
2ND NETWORK
150
140
TCA
B
170
I/O UNIT
LINK
LINK
130
100'
160
A
HCA
LINK
LINK
MULTI-
STAGE
SWITCH
LINK
LINK
TCA
HOST SYSTEM
120
LINK
C
LINK
180
TCA
D
190
250
CENTRAL
NETWORK
MANAGER
REMOTE SYSTEM

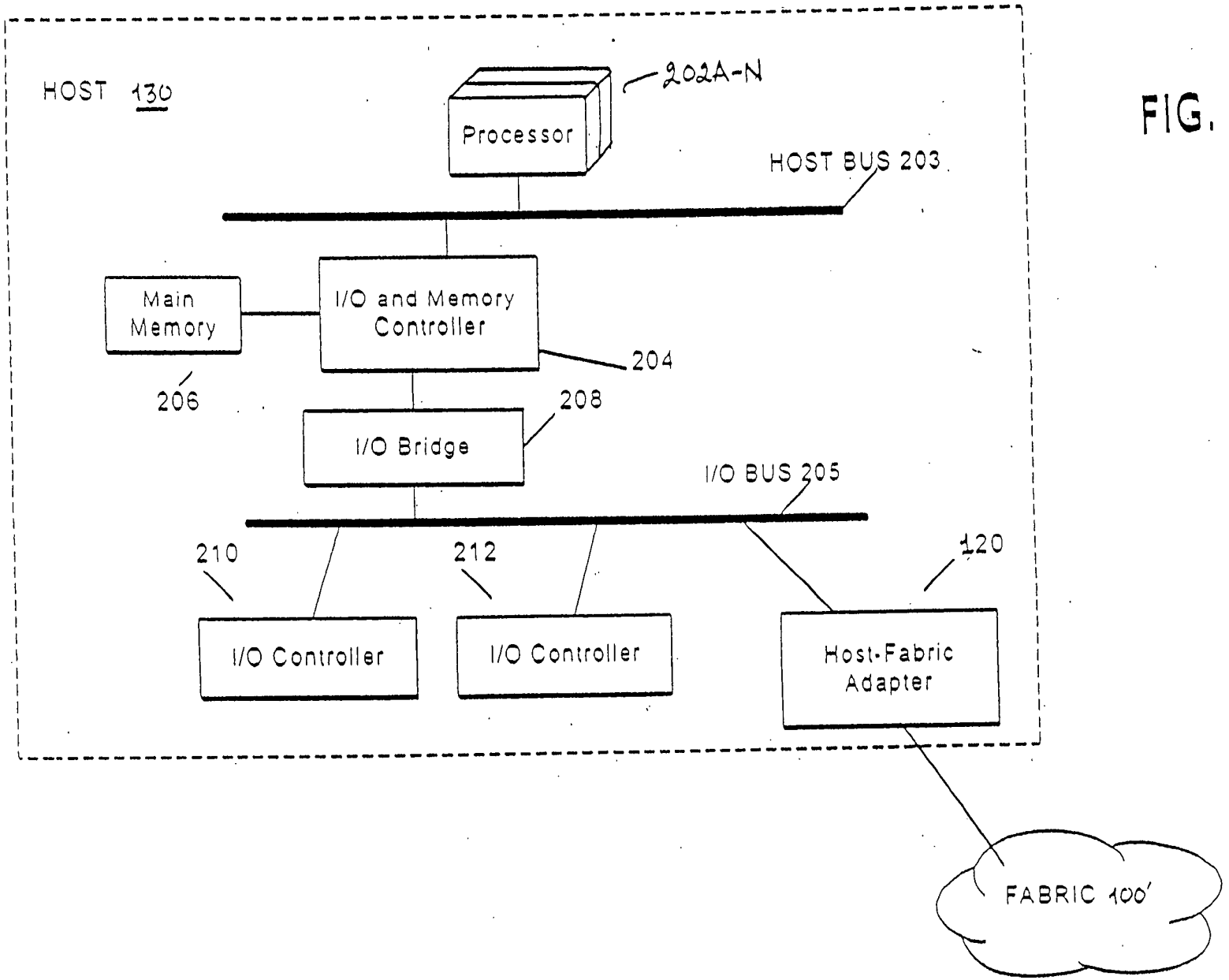

HOST 130
Processor
202A-N
HOST BUS 203
Main Memory
I/O and Memory Controller
204
206
208
I/O Bridge
I/O BUS 205
210
212
120
I/O Controller
I/O Controller
Host-Fabric Adapter
FABRIC 100'

FIG. 4A

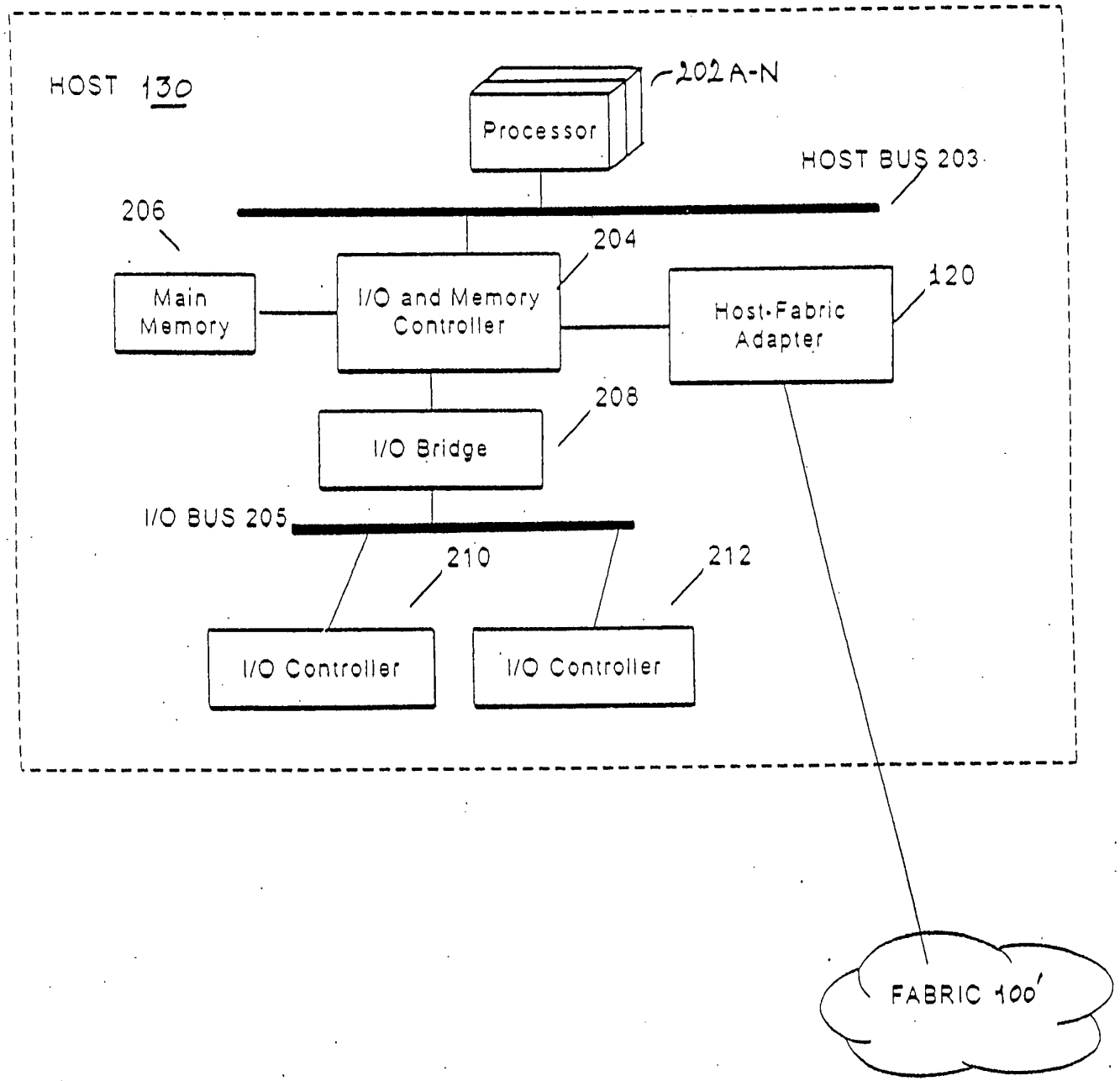
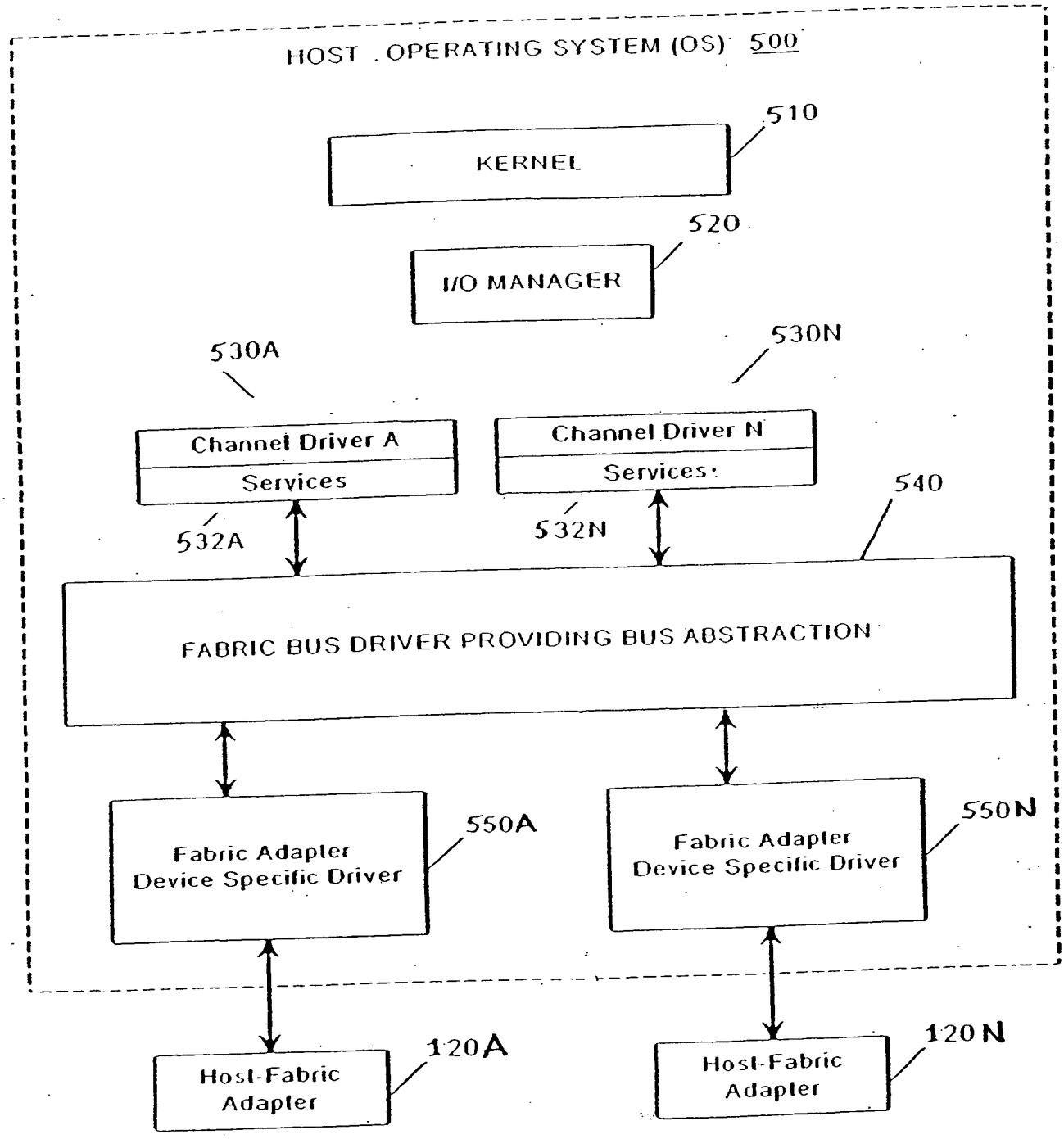

HOST 130
202 A-N
Processor
HOST BUS 203
206
204
Main Memory
I/O and Memory Controller
120
Host-Fabric Adapter
208
I/O Bridge
I/O BUS 205
210
212
I/O Controller
I/O Controller
FABRIC 100'

FIG. 4B



EXAMPLE SOFTWARE DRIVER STACKS OF HOST SYSTEM

FIG. 5

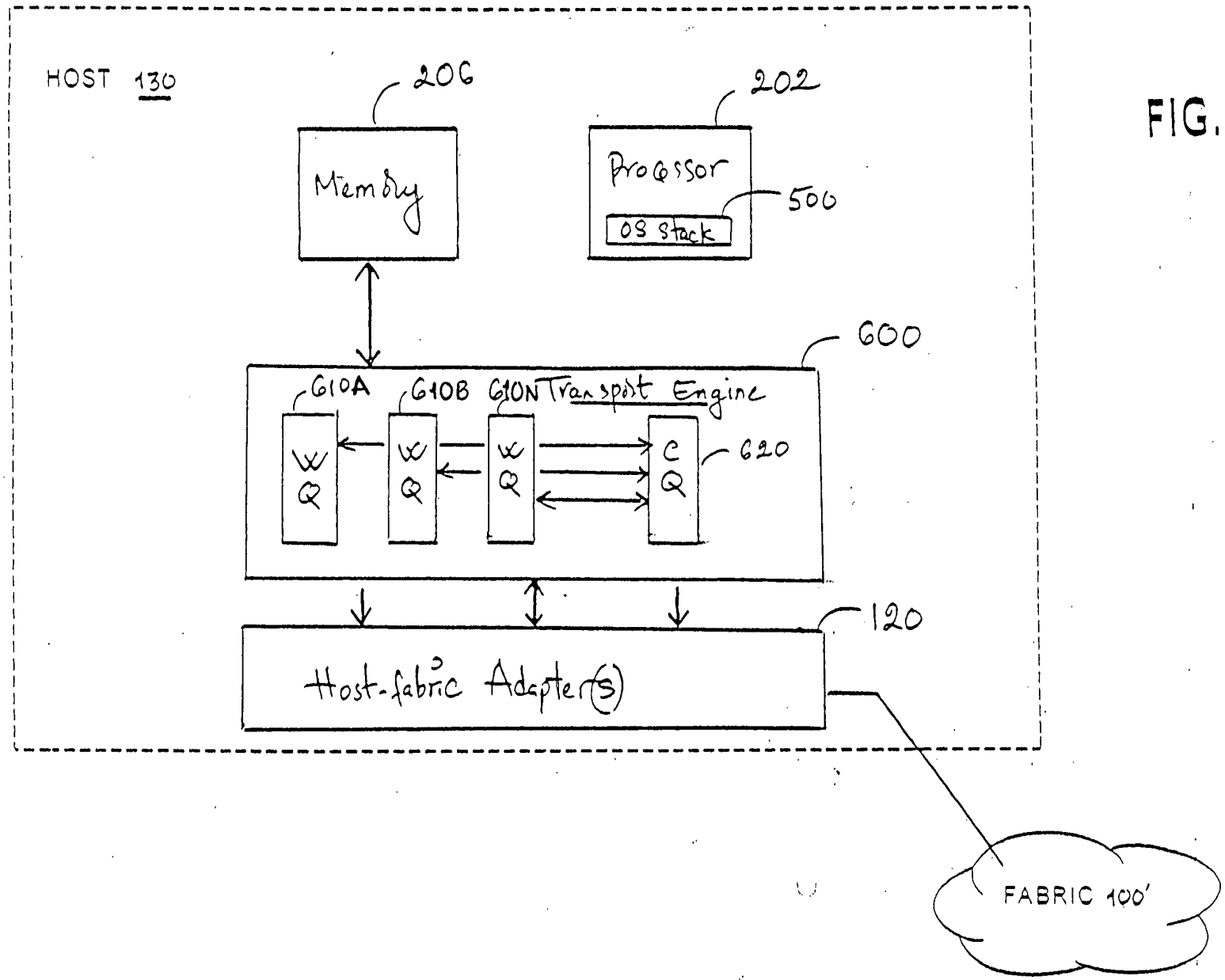

HOST 130
206
Memory
202
Processor
500
OS Stack
600
610A
610B
610N Transport Engine
WQ
WQ
WQ
CQ
620
120
Host-fabric Adapter(s)
FABRIC 100'

FIG. 6

FIG. 7

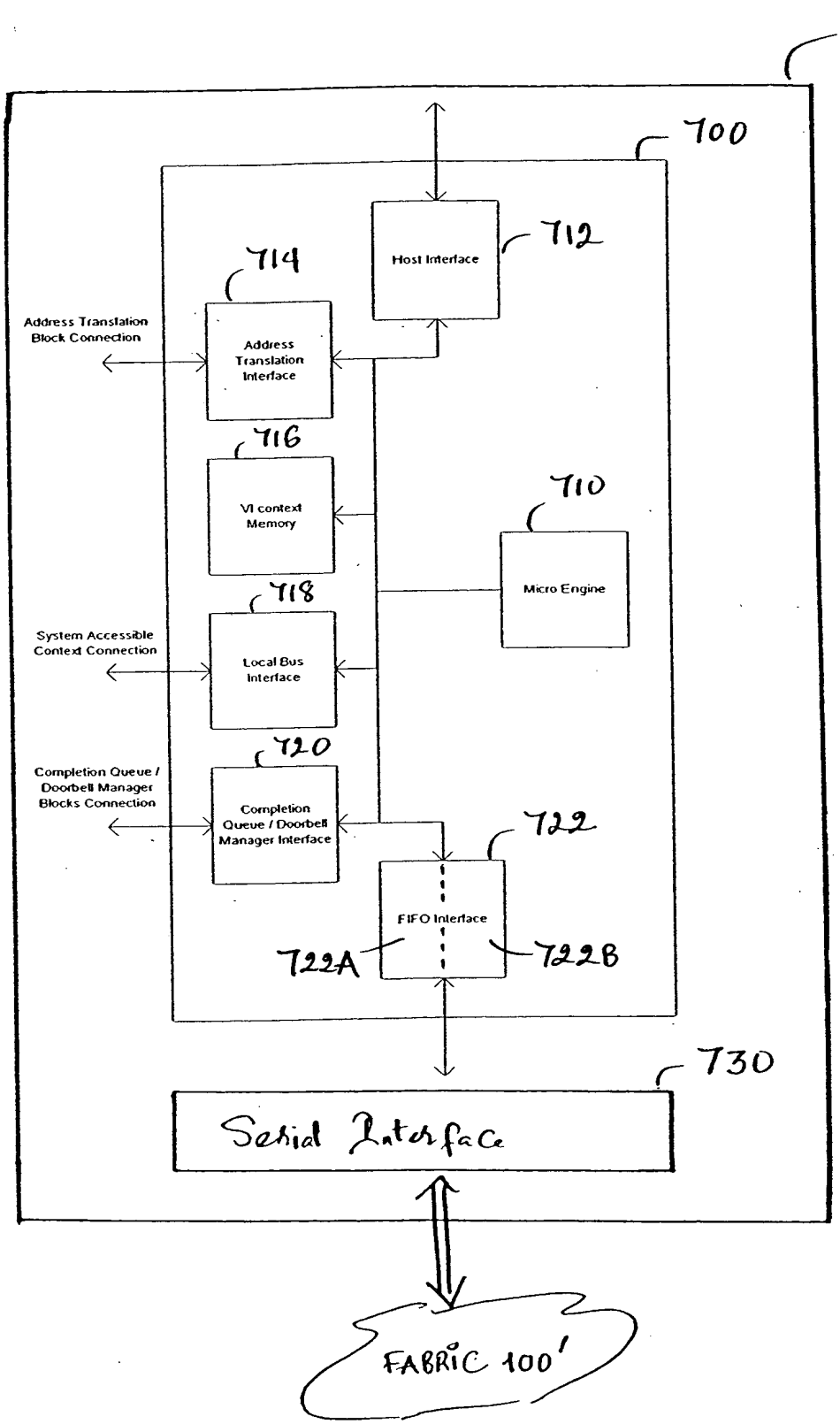

120
700
Host Interface
712
714
Address Translation Block Connection
Address Translation Interface
716
VI context Memory
710
Micro Engine
718
System Accessible Context Connection
Local Bus Interface
720
Completion Queue / Doorbell Manager Blocks Connection
Completion Queue / Doorbell Manager Interface
722
FIFO Interface
722A
722B
730
Serial Interface
FABRIC 100'

FIG. 8

710

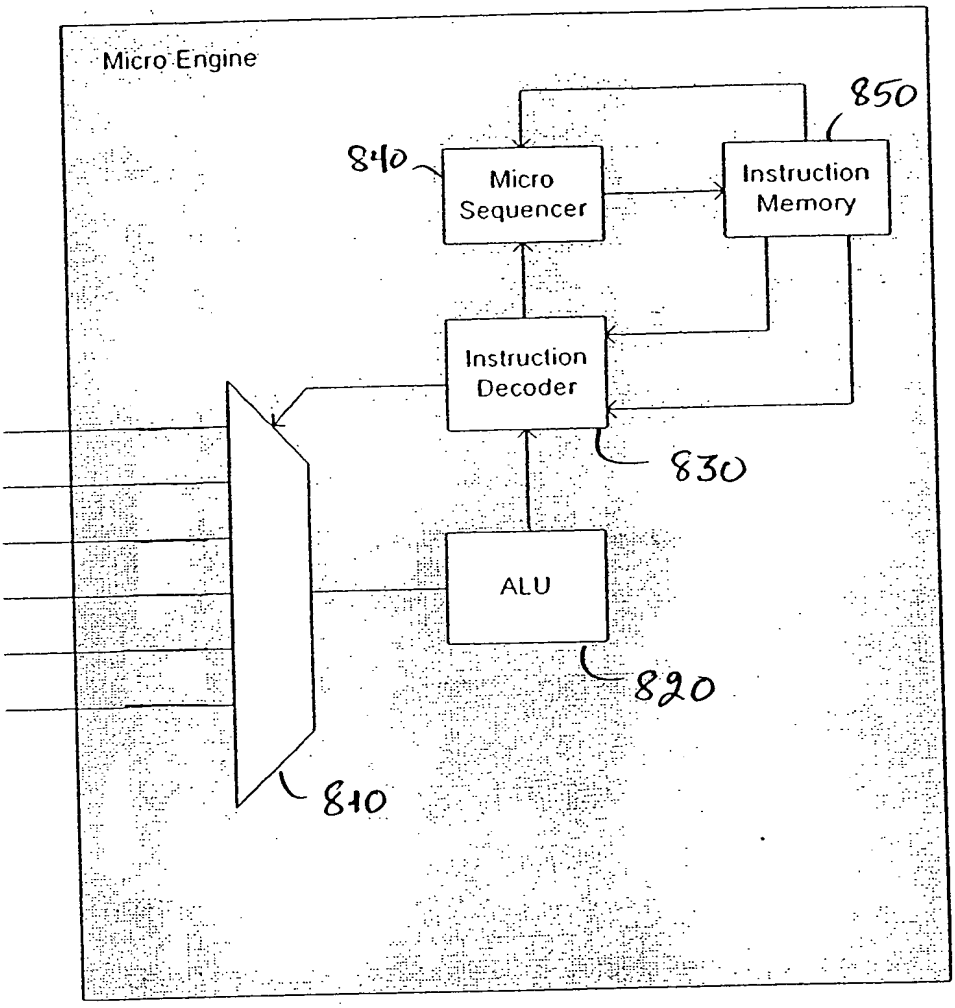

Micro Engine
850
840
Micro Sequencer
Instruction Memory
Instruction Decoder
830
ALU
820
810

FIG. 9

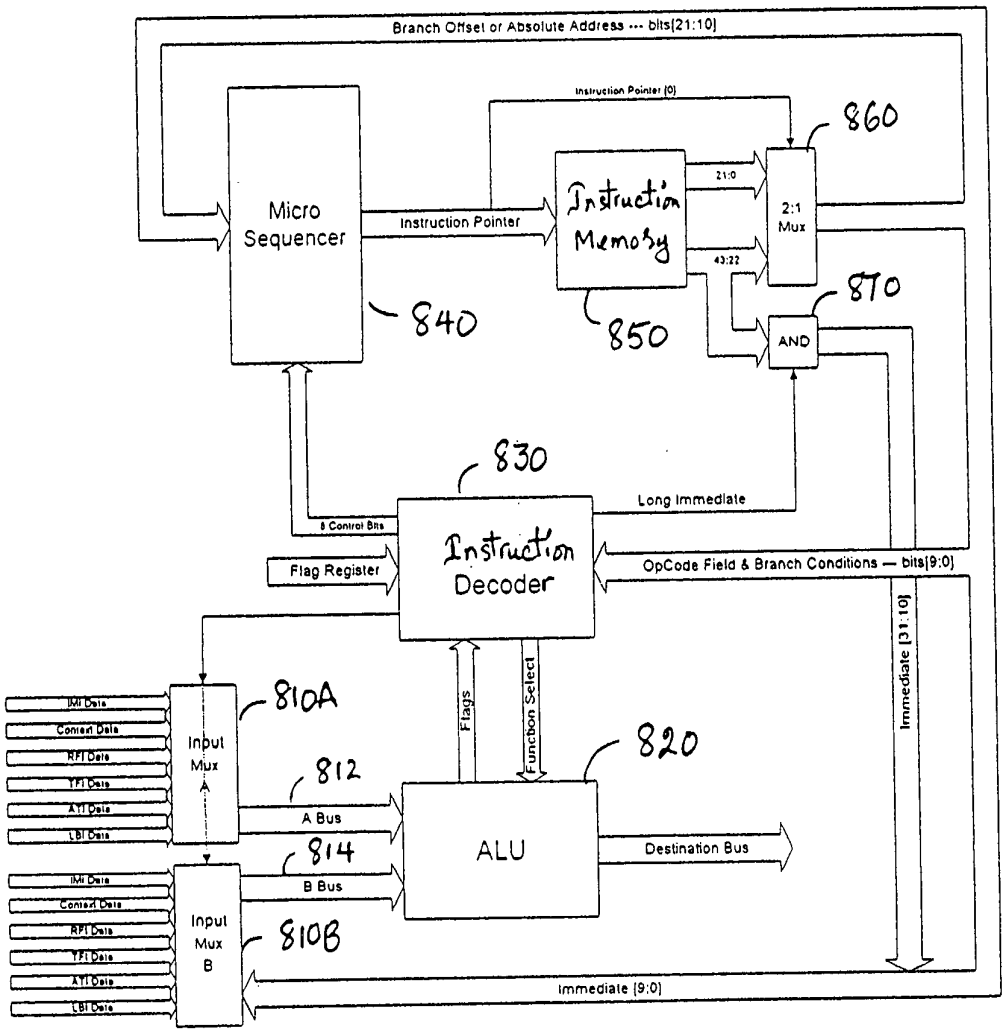
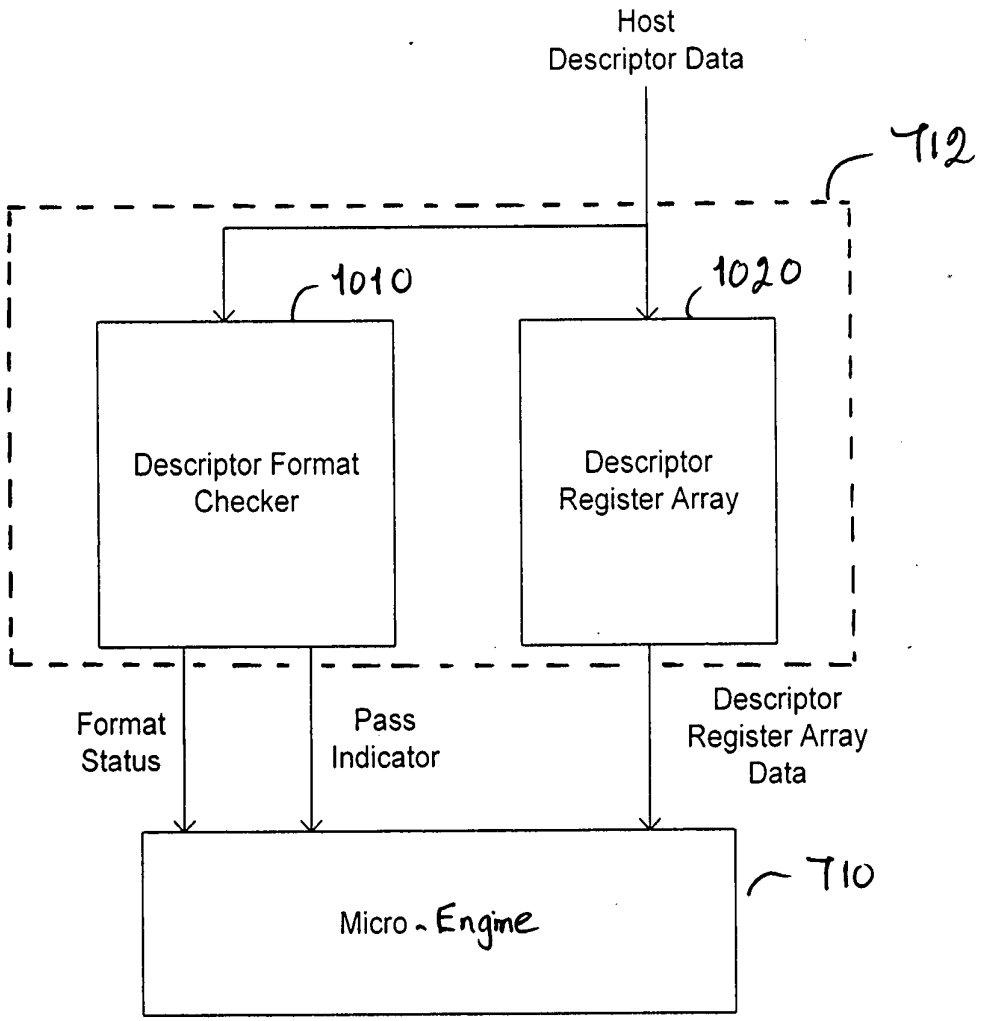

710
Branch Offset or Absolute Address --- bits[21:10]
Instruction Pointer [0]
860
Micro Sequencer
Instruction Pointer
Instruction Memory
21:0
43:22
2:1 Mux
870
AND
840
850
830
Long Immediate
8 Control Bits
Flag Register
Instruction Decoder
OpCode Field & Branch Conditions — bits[9:0]
Immediate [31:10]
Flags
Function Select
810A
Input Mux A
IMI Data
Context Data
RFI Data
YFI Data
AYI Data
LBI Data
812
A Bus
814
B Bus
820
ALU
Destination Bus
Input Mux B
810B
Immediate [9:0]

FIG. 10


Host
Descriptor Data
712
1010
1020
Descriptor Format
Checker
Descriptor
Register Array
Format
Status
Pass
Indicator
Descriptor
Register Array
Data
710
Micro - Engine

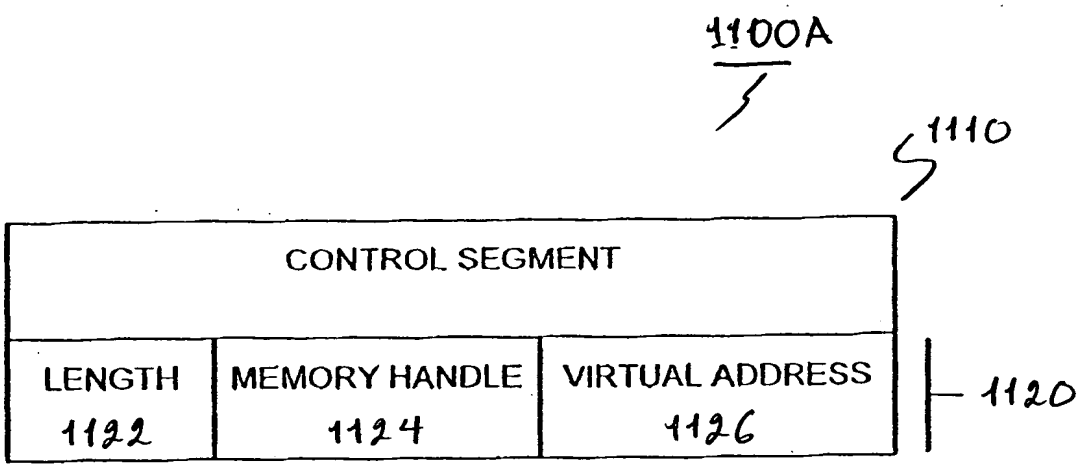


FIG.11A

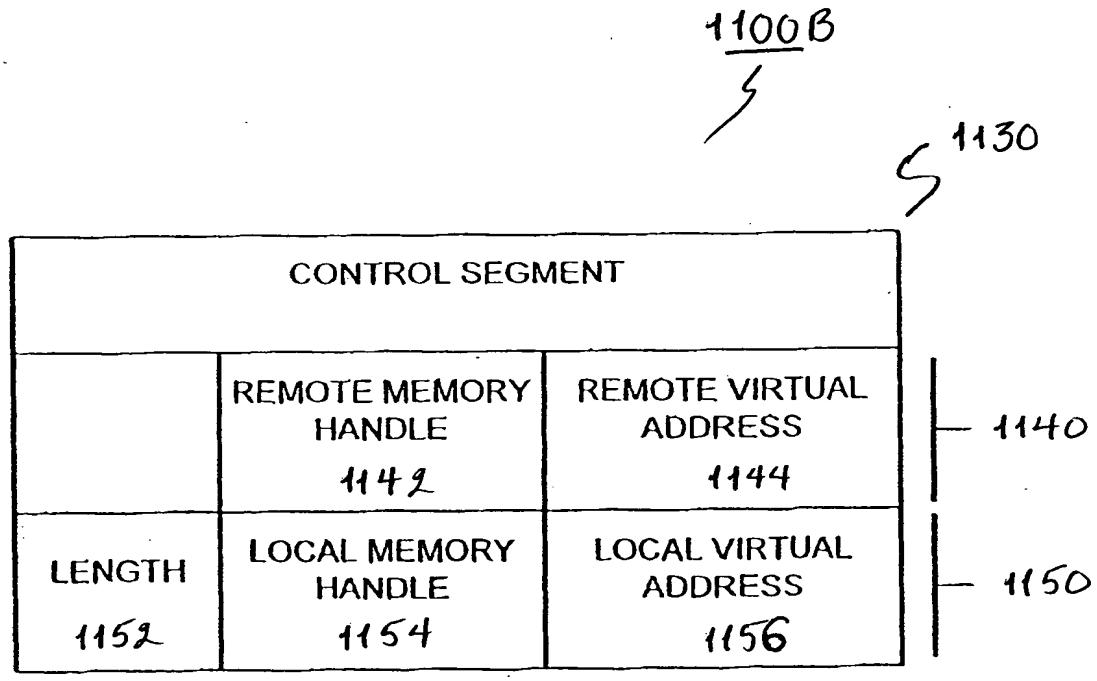


FIG.11B

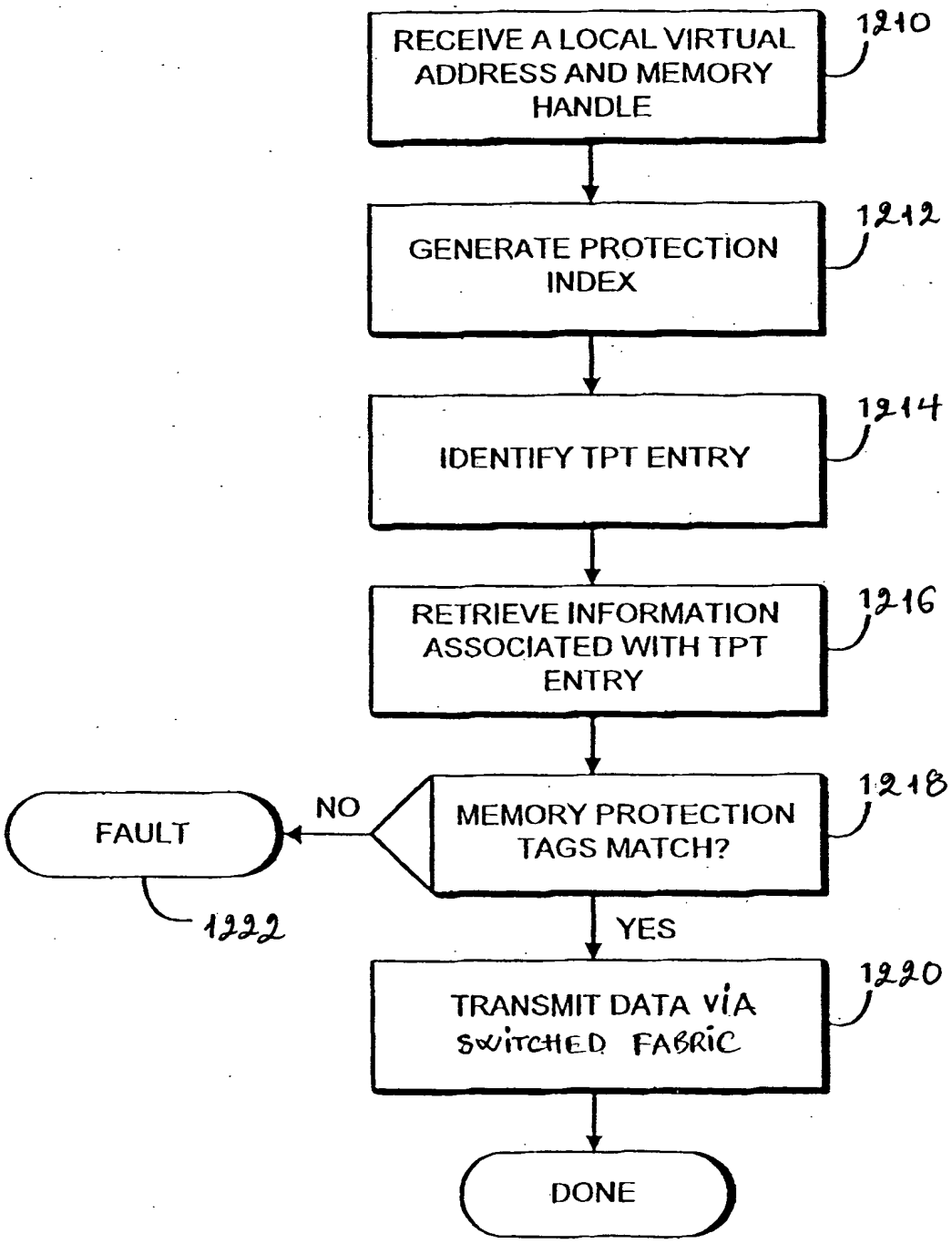

RECEIVE A LOCAL VIRTUAL ADDRESS AND MEMORY HANDLE
1210
GENERATE PROTECTION INDEX
1212
IDENTIFY TPT ENTRY
1214
RETRIEVE INFORMATION ASSOCIATED WITH TPT ENTRY
1216
MEMORY PROTECTION TAGS MATCH?
1218
NO
FAULT
1222
YES
TRANSMIT DATA VIA SWITCHED FABRIC
1220
DONE

FIG. 12

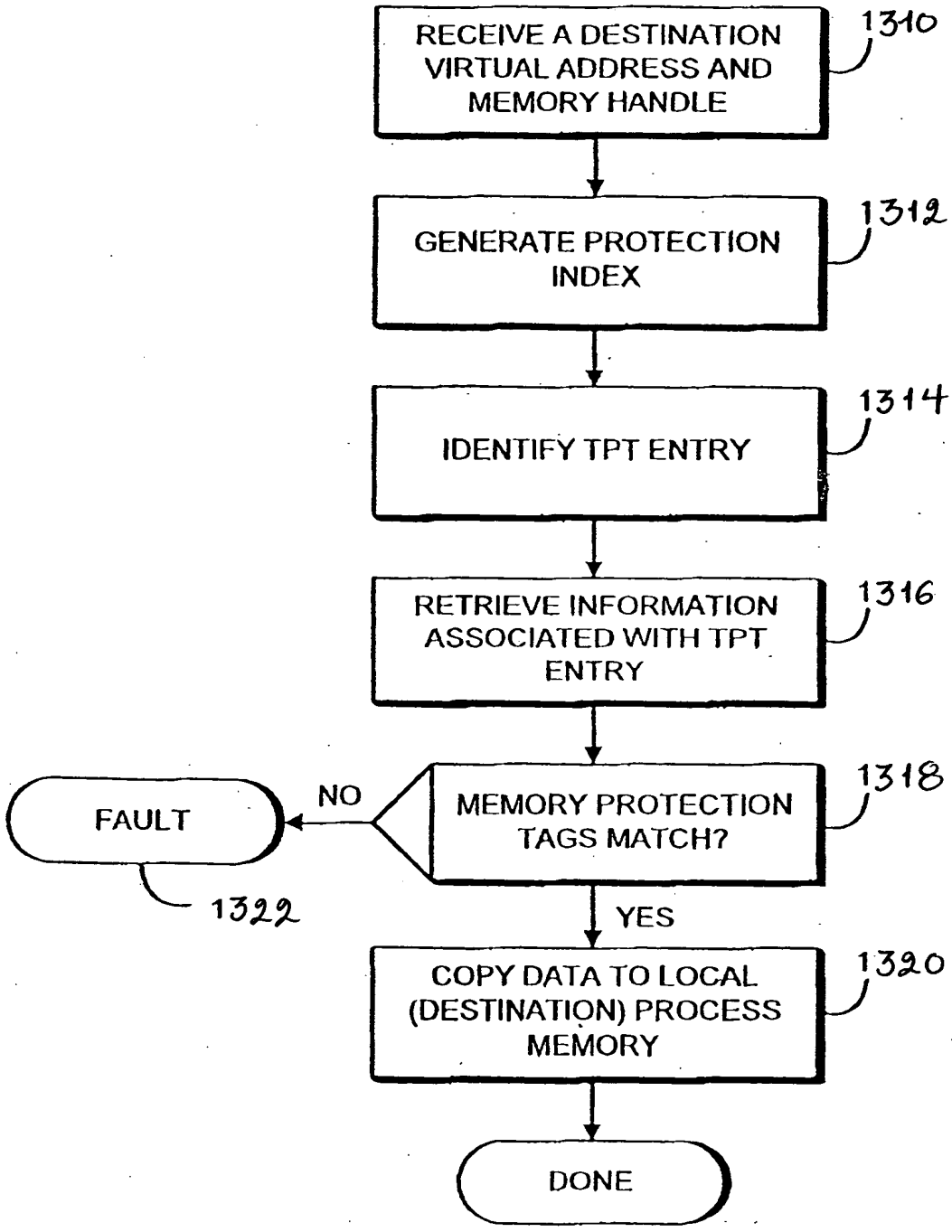

RECEIVE A DESTINATION VIRTUAL ADDRESS AND MEMORY HANDLE
1310
GENERATE PROTECTION INDEX
1312
IDENTIFY TPT ENTRY
1314
RETRIEVE INFORMATION ASSOCIATED WITH TPT ENTRY
1316
MEMORY PROTECTION TAGS MATCH?
1318
NO
FAULT
1322
YES
COPY DATA TO LOCAL (DESTINATION) PROCESS MEMORY
1320
DONE

FIG. 13

FIG. 14

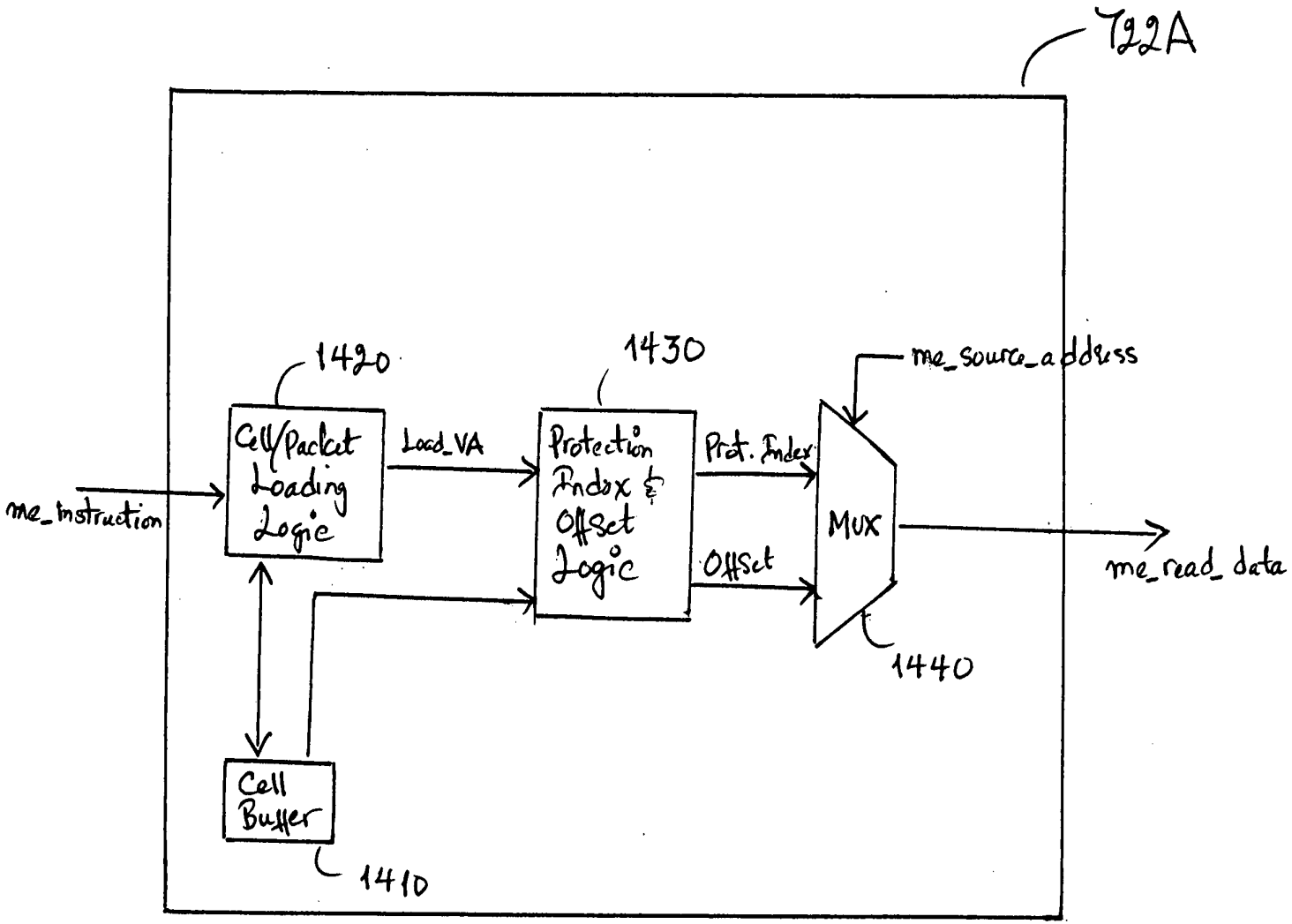

722A
1420
1430
me_source_address
Cell/Packet Loading Logic
Load_VA
Protection Index & Offset Logic
Prot. Index
Offset
MUX
me_instruction
me_read_data
1440
Cell Buffer
1410

FIG. 15

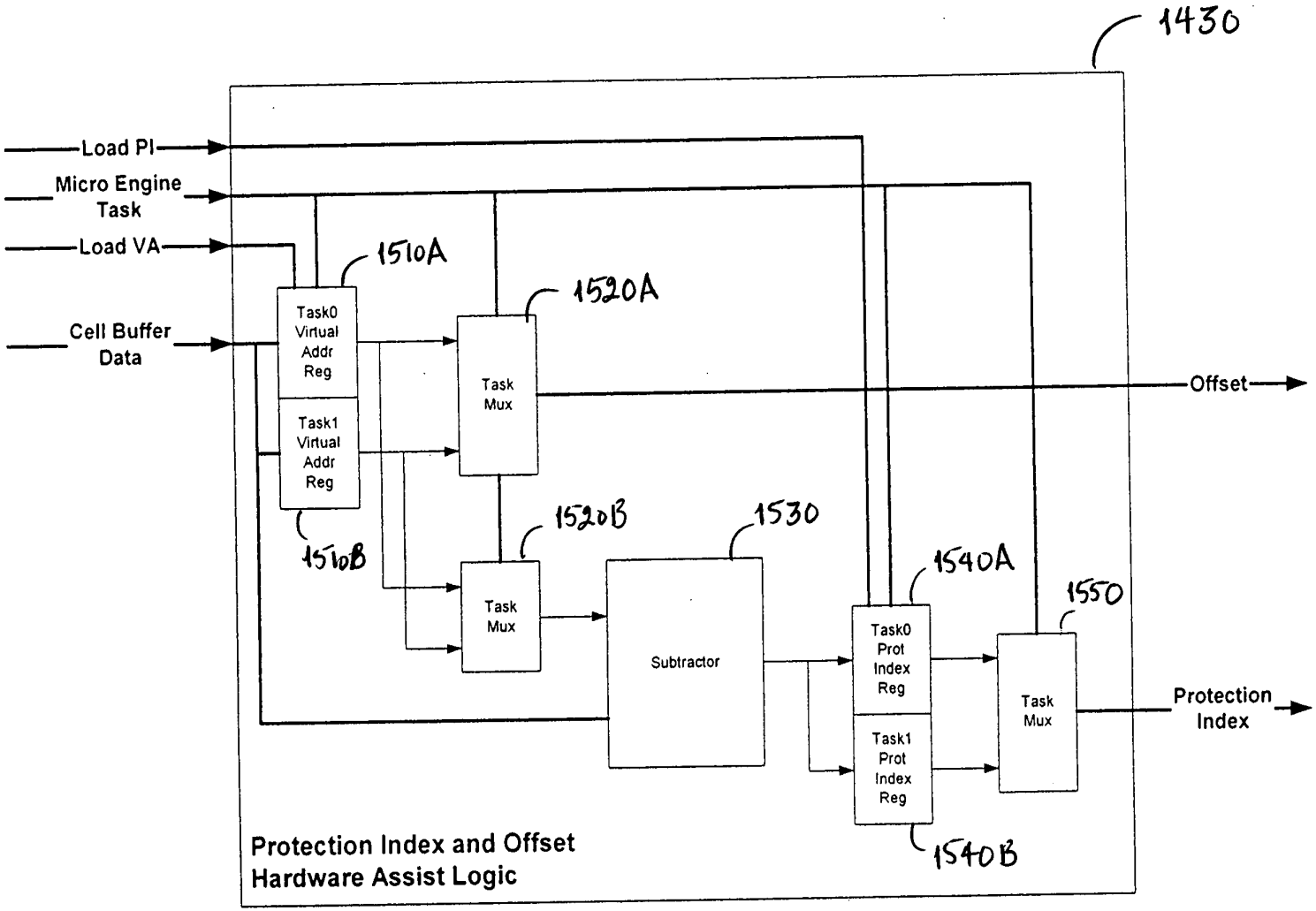
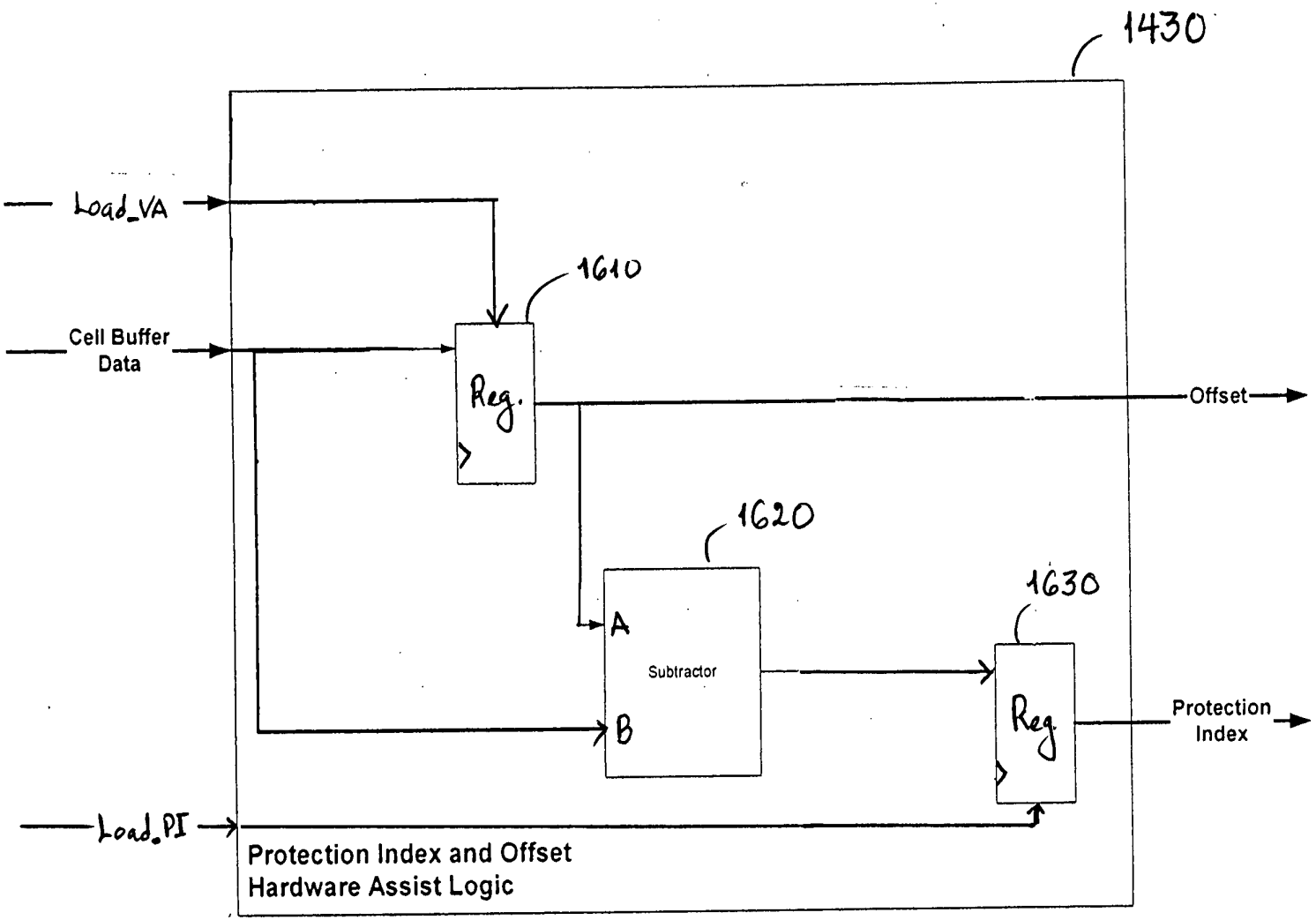

1430
Load PI
Micro Engine Task
Load VA
Cell Buffer Data
1510A
Task0 Virtual Addr Reg
Task1 Virtual Addr Reg
1510B
1520A
Task Mux
1520B
Task Mux
1530
Subtractor
1540A
Task0 Prot Index Reg
Task1 Prot Index Reg
1540B
1550
Task Mux
Offset
Protection Index
Protection Index and Offset Hardware Assist Logic

FIG. 16


1430
Load_VA
1610
Cell Buffer Data
Reg.
Offset
1620
1630
A
Subtractor
B
Reg
Protection Index
Load_PI
Protection Index and Offset Hardware Assist Logic

FIGs. 17A-17H

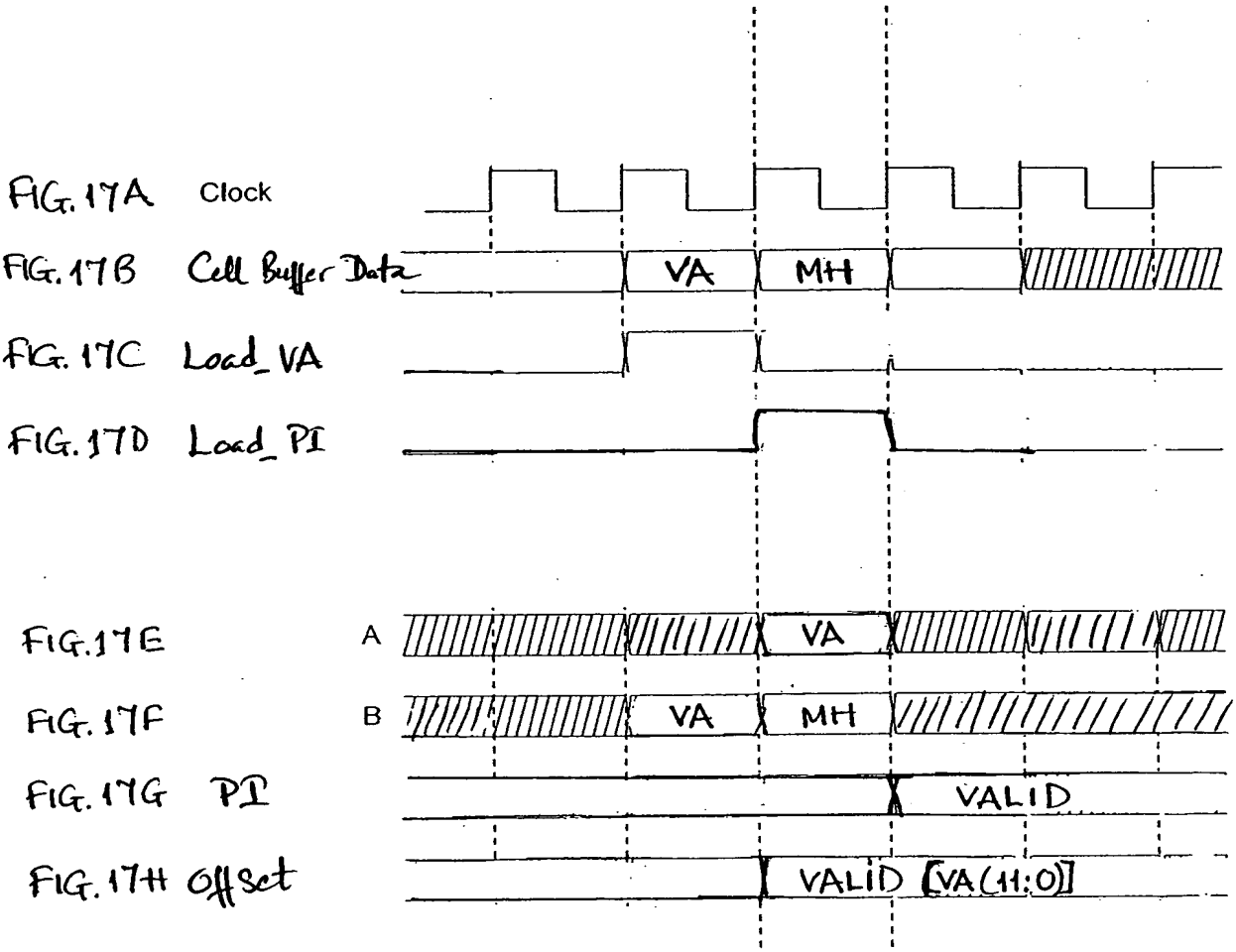


FIG. 17A Clock
FIG. 17B Cell Buffer Data
VA
MH
FIG. 17C Load_VA
FIG. 17D Load_PI
FIG. 17E
A
VA
FIG. 17F
B
VA
MH
FIG. 17G PI
VALID
FIG. 17H Offset
VALID [VA(11:0)]